- This document will guide you through compiling and testing the provided mcx16 demonstration code on the Avnet Spartan-6 LX9 MicroBoard. The code was tested using Xilinx ISE 13.2.
- The MicroBoard is inexpensive (\$89 when I bought one), but even if you don't have one you can still use the provided sample code to experiment with synthesizing the mcx16 microcontroller.

mcx16 is a 16-bit microcontroller written in VHDL. It was inspired by PicoBlaze, an 8-bit microcontroller designed by Ken Chapman at Xilinx. mcx16 uses an instruction set and architecture similar to PicoBlaze, so if you've already learned one, using the other should be straightforward. The mcx16 code is tested on Xilinx FPGAs.

Some highlights of mcx16:

- 16-bit addresses, data, port addresses and ports
- Can use 1 (non-pipelined) or 2 (pipelined) clocks per instruction
- 74MHz (74 MIPS) on a Spartan 3 XC3S200AN-4 non-pipelined, and 119 MHz when pipelined (59 MIPS), using 110/114 slices (area optimized, 16 registers, 32 deep stack, 512 word program, distributed stack)
- 107 MHz (107 MIPS) on a Spartan 6 XC6SLX9-2 non-pipelined, and 166 MHz when pipelined (83 MIPS), using 46/41 slices
- Pipelining, register count (1 256), stack depth (1 65536), and program/stack type (BRAM/distributed) are all user-set generics; program size up to 65536 words
- Cross-platform assembler
- Optional JTAG loader using Kris Chaplin's technique and cross-platform Xilinx tools

Source Files

- mcx16s6mb.xise:
- mcx16s6mb.vhd:
- mcx16s6mb.ucf:
- mcx16.vhd:
- mcx16s6mb_rom.txt:
- mcx16s6mb_rom.vhd:
- mcx16loader.vhd:
- mcx16uart.vhd:
- mcx16util.vhd:

Project file Top level VHDL Pin and clock constraints Microcontroller VHDL **Program ROM source Program ROM VHDL** JTAG loader VHDL UART VHDL Shared utility VHDL



SETUP

- Extract the mcx16s6mb.zip file into a directory
- Open the mcx16s6mb.xise project file with ISE
- Let it create a "work" directory if prompted
- Double-click "Generate Programming File"
- This should complete without errors
- Click the "Design Summary" button to inspect the design's resource usage

COMPILE PROJECT

> ISE Project Navigator (0.61xd) - D:\mcx16\mcx16s6mb\mcx16s6mb.xise - [Design Summary]					
∑ Elle Edit Yiew Project Source Process Tools Window Layout Help					
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Design ↔ □ ₽ ×	Mum	mber of occupied Slices 83	1,430 5%		
View: 💿 🔯 Implementation 🔿 🔝 Simulation	IOB Properties	mber of LUT Flip Flop pairs used 272			
Hierarchy	Module Level Utilization	Number with an unused Flip Flop 148	272 54%		
a mcx16s6mb	Iming Constraints Pipout Report	Number with an unused LUT 50	272 18%		
E Costo - 2000 -	Clock Report	Number of fully used LUT-FF pairs 74	272 27%		
	Static Timing	Number of unique control sets 26			
	Image: Synthesis Messages N	Number of slice register sites lost 129 to control set restrictions	11,440 1%		
	Translation Messages	mber of bonded IOBs 4	200 2%		
	Map Messages	Number of LOCed IOBs 4	4 100%		
	Timing Messages	IOB Flip Flops 2			
	Bitgen Messages Num	mber of RAMB16BWERs 1	32 3%		
No Processes Running	All Implementation Messages	mber of RAMB8BWERs 0	64 0%		
Processes: mcx16s6mb - Behavioral	Synthesis Report	mber of BUFIO2/BUFIO2_2CLKs 0	32 0%		
Design Summary/Reports	Translation Report	mber of BUFIO2FB/BUFIO2FB_2CLKs 0	32 0%		
Design Utilities	Design Properties Num	mber of BUFG/BUFGMUXs 2	16 12%		
Constraints Constraints Constraints Constraints Constraints	Optional Design Summary Contents	Number used as BUFGs 2			
💶 🗄 🚺 Implement Design	Show Clock Report	Number used as BUFGMUX 0			
Configure Target Device	Show Warnings	mber of DCM/DCM_CLKGENs 0	4 0%		
Analyze Design Using ChipScope	Show Errors	mber of ILOGIC2/ISERDES2s 1	200 1%		
	N	Number used as ILOGIC2s 1			
	N	Number used as ISERDES2s 0			
Start 🗈 Design 🗈 Files 📭 Libraries	Design Summary		1 1		
Console ↔ □ ♂ ×					
Command Line: bitgen -intstyle ise -f mcx1656	b.ut mcx16s6mb.ncd /ty fife/Mrem fife1 PAMD D1 ON is			<u> </u>	
VARNINC: PhysDesignRules: 367 - The signal <uart hram_titol_kamp_d1_05="" is<="" td="" tx_tito=""></uart>					
LUARNING:PhysDesignRules:367 - The signal <uart mram_fifo1_ramd_d1_o="" rx_fifo=""> is</uart>					
incomplete. The signal does not drive any load pins in the design.					
1) INFO: WebTalk: 4 - D:/mcx16/mcx16s6mb/work/usage statistics webtalk.html WebTalk					
report has been successfully sent to Xilinx. For additional details about this					
file, please refer to the WebTalk log file at D:/mcx16/mcx16s6mb/work/webtalk log					
D., MCXIO, MCXIOSOMD, WOLK, WCDCulk. Tog					
WebTalk is complete.					
Process "Generate Programming File" completed successfully					
Launching Design Summary/Report Viewer					
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📋 Console 😂 Errors 🚣 Warnings 😹 Find in Files Results					
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LAUNCH IMPACT

- It is assumed that you've already installed the Digilent JTAG drivers for the MicroBoard, along with the Silicon Labs CP2102 serial port drivers (these steps are described in detail in the MicroBoard documentation)
- With the MicroBoard connected to your computer (both through the microUSB connector for serial and through the full USB connector for JTAG), launch iMPACT, create a new project, and assign the work/mcx16s6mb.bit file to the FPGA

ASSIGN BIT FILE



PROGRAM AND TEST

- Open a serial terminal to the MicroBoard (using HyperTerm, PuTTY, etc, 115200 N81)
- Program the MicroBoard with the bit file
- You should see "Hello World!" after programming, and every time you press the reset switch on the MicroBoard (SW5)
- When you type into the terminal, it should respond with the two digit hex codes of the characters you typed (programmed, typed "ABC" and then pressed SW5 in the following screen)

TERMINAL OUTPUT



EXPERIMENT

- Download the mcx16 files (which includes the assembler) into a directory, and copy the "mcx16s6mb_rom.txt" file into the same directory
- Launch the "ISE Design Suite Command Prompt" and navigate to the directory with the mcx16 files
- Edit the "mcx16s6mb_rom.txt" file (change the 'H' to 'J' in "Hello World", for example), and then run:
 mcx16asm mcx16s6mb_rom.txt -1
- This will compile and load the new code via JTAG into the mcx16rom, and restart the processor



EXPERIMENT

👞 ISE Design Suite Command Prompt	
D:\mcx16>mcx16asm mcx16s6mb_rom	.txt -1
=== mcx16 Assembler R1 ===	
Assembly successful. Highest address used: 43 (0x2B) ROM size: 512 (0x200). Starting impact Program successfully uploaded.	
D:\mex16\	
D. (((C)10)_	Hello World!
	42
	43
	Hello World!
	Hello World!
	Jello World!
	·

CONCLUSION

- This concludes the quick mcx16 demo. Feel free to experiment - compare resource usage for different numbers of registers, stack depths, single/dual cycle, or check maximum clock frequencies (> 111 MHz for the example single cycle project).
- Thanks for giving mcx16 a try, I hope it proves useful! The latest mcx16 info will be posted at

http://www.bitpond.com/mcx16